MHL Bridge with Embedded Controller

EP94M1E

Data Sheet

V0.5

Original Release Date: Oct. 26, 2011
Revised Date: May 21, 2012

Explore

Revision History

Version Number	Revision Date	Author	Description of Changes
0.1	Oct/26/2011	Ether Lai	Initial Version
0.2	Nov/11/2011	Ether Lai	Redefine the User Guide to Data Sheet; Revised the Package Information (LQFP to QFN); Add the CBUS I/O Specification
0.3	Mar/16/2012	Ether Lai	Fix the typo in pin description;
0.4	Apr/30/2012	Ether Lai	Revise the Electrical Characteristics;
0.5	May/21/2012	Ether Lai	Revise the footprint diagram;

Section 1 Introduction

1.1 Overview

EP94M1E is a MHL Receiver with HDMI output and embedded MCU. The chip is compliant with HDMI 1.4b and MHL 1.2 specifications. The chip supports the resolution up to 720p 60 Hz, 1080p 30 Hz or 1080p 60Hz in PackedPixel Mode. The chip also supports on-chip EDID RAM and programmable passive/active DDC switches to lower down system cost and provide the flexibility for the EDID handling. With an embedded MCU on-chip, the chip does not require external MCU to support the RAP/RCP and CEC function. User is not required to develop the software.

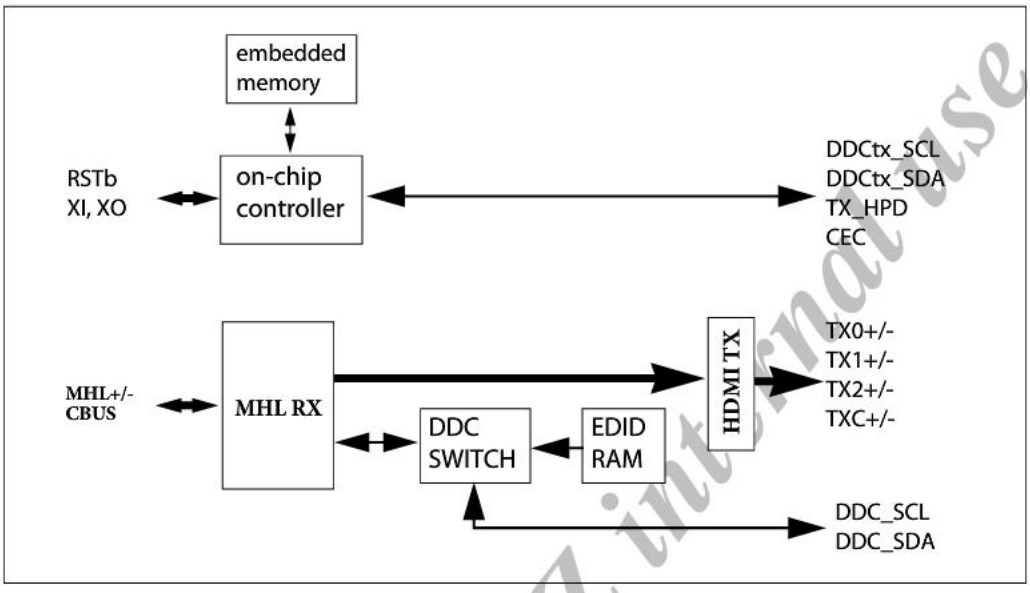
1.2 Features

- On-chip embedded MCU. No external MCU is required to support the RAP/RCP and CEC function. No software development is required.
- On-chip MHL Receiver and HDMI Transmitter core which are compliant with MHL 1.1 and HDMI 1.4b specification
- On-chip MHL/HDMI Bridge with Equalizer
- Supports 1 MHL input port and 1 HDMI output port
- Support up to 75 Mhz Pixel clock rate (8-bit 720p 60 Hz or 1080p 30Hz)
- Support up to 148.5 Mhz Pixel clock rate in PackedPixel Mode(8-bit 1080p 60 Hz)
- Support on-chip EDID RAM
- Support on-chip programmable passive/active DDC switches
- Support the RAP/RCP Function
- Support the CEC Function
- Low stand-by current (< 1mA) at power down mode
- Pin compatible to EP94M0E
- 48-pin QFN package

Section 2 Overview

2.1 Chip Block Diagram

Figure 2-1 Block Diagram



2.2 Pin Diagram

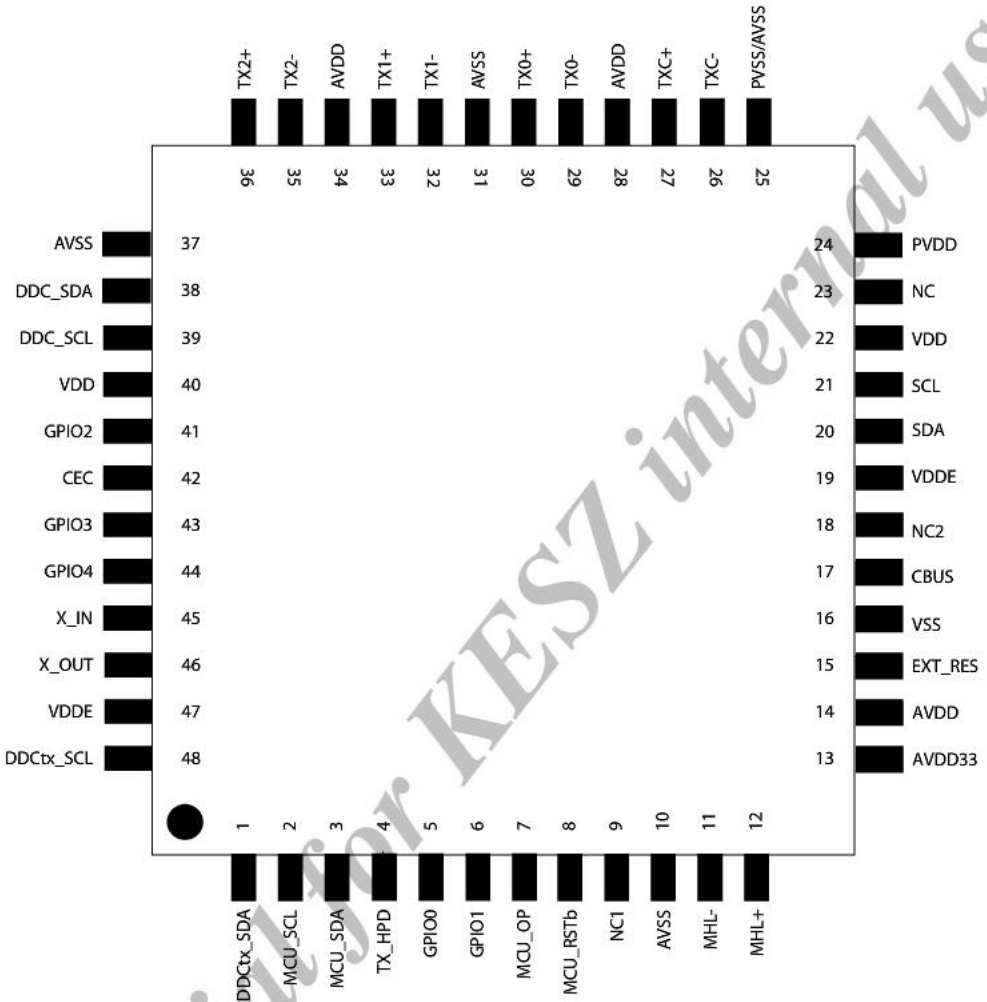


Figure 2-2 Pin Diagram

2.3 Pin Description

Unless otherwise stated, unused input pins must be tied to ground, and unused output pins left open.

Table 2-1 MHL Input Port

Name	In/Out	Description
MHL-	IN	Differential Data Input Pair0 for MHL Input Port
MHL+	IN	Differential Data Input Pair0 for MHL Input Port
CD_SENSE	IN	MHL Cable Detect.
CBUS	IO	CBUS signal for MHL RX Port
EXT_RES	IN	External Termination Resistor for HDMI Input Port. A resistor should tie this pin to AVDD33. 510Ω is recommended.

Table 2-2 HDMI Output Ports

Name	In/Out	Description
TXC-	OUT	Differential Clock Output Pair for HDMI Output
TXC+	OUT	Differential Clock Output Pair for HDMI Output
TX0-	OUT	Differential Data Output Pair0 for HDMI Output
TX0+	OUT	Differential Data Output Pair0 for HDMI Output
TX1-	OUT	Differential Data Output Pair1 for HDMI Output
TX1+	OUT	Differential Data Output Pair1 for HDMI Output
TX2-	OUT	Differential Data Output Pair2 for HDMI Output
TX2+	OUT	Differential Data Output Pair2 for HDMI Output

Table 2-3 IIC & MCU Interface

Name	In/Out	Description
DDC_SCL/DDCtx_SCL	IO	IIC SDA signal for HDMI TX DDC Port
DDC_SDA/DDCtx_SDA	IO	IIC SCL signal for HDMI TX DDC Port;
SCL/MCU_SCL	IO	SCL signal for on-chip controller; Shall be connected together with external 2KΩ pull-up resistor;
SDA/MCU_SDA	IO	SDA signal for on-chip controller; Shall be connected together with external 2KΩ pull-up resistor;
TX_HPD	IN	Hot Plug Detect Input from HDMI Output Connector
GPIO0	IO	GPIO0;
GPIO1	IO	GPIO1;
MCU_OP	IN	On-chip Controller operation mode. 0: Normal mode 1: ICP (In Circuit Flash Programming) mode
MCU_RSTb	IN	External Reset input (Active Low) with internal weak pull-up.
NC1/NC2	IO	Leave these pins unconnected in normal operation
GPIO2	IO	GPIO 2 (Open Drain);
CEC	IO	CEC I/O pin

Table 2-3 IIC & MCU Interface

Name	In/Out	Description
XI	IN	External Crystal Input, 24 Mhz
XO	OUT	External Crystal Output, 24 Mhz.

Table 2-4 Power Pins

Name	In/Out	Description
AVDD	PWR	MHL/HDMI RX/TX Analog Power (1.8V)
PVDD	PWR	MHL/HDMI RX/TX PLL Analog Power (1.8V)
AVDD33	PWR	MHL/HDMI Termination Power (3.3V)
VDDE	PWR	I/O Power (3.3V)
VDD	PWR	Internal Logic Power (1.8V)
VSS	GND	Common Ground

2.4 Electrical Characteristics

Absolute Maximum Conditions

Symbol	Parameter	Min	Typ	Max	Units
Vcc33	3.3V Supply Voltage	-0.3		4.0	V
Vcc18	1.8V Supply Voltage	-0.3		2.5	V
V_I	Input Voltage	-0.3		$V_{cc33}+0.3$	V
V_O	Output Voltage	-0.3		$V_{cc33}+0.3$	V
T_J	Junction Temperature			125	°C
T_{STG}	Storage Temperature	-40		125	°C
θ_{JA}	Thermal Resistance (Junction to Ambient)		60		°C/W
θ_{JC}	Thermal Resistance (Junction to Case)		17		°C/W

Normal Operating Conditions

Symbol	Parameter	Min	Typ	Max	Units
Vcc33	3.3V Supply Voltage	3.14	3.3	3.6	V
Vcc18	1.8V Supply Voltage	1.71	1.8	1.98	V
V_{CCN}	Supply Voltage Noise[1]	-0.3		100	mV_{p-p}
T_A	Ambient Temperature (with power applied)	0	25	70	°C

DC Digital I/O Specifications (under normal operating conditions unless otherwise specified)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{IH}	High-level Input Voltage		2.0			V
V_{IL}	Low-level Input Voltage				0.8	V
V_{OH}	High-level Output Voltage		2.4			V
V_{OL}	Low-level Output Voltage				0.4	V
I_{OL}	Output Leakage Current	High Impedance	-10		10	uA

CBUS I/O Specifications (under normal operating conditions unless otherwise specified)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{IH_CBUS}	CBUS High-level Input Voltage		1.0			V
V_{IL_CBUS}	CBUS Low-level Input Voltage				0.6	V
V_{OH_CBUS}	CBUS High-level Output Voltage	VDD = 1.8V	1.5		1.9	V
V_{OL_CBUS}	CBUS Low-level Output Voltage				0.2	V
I_{IH_CBUS}/I_{IL_CBUS}	Input Leakage Current	High Impedance	-1		1	uA
$Z_{CBUS\_SINK\_DISCOVER}$	CBUS Pull Down Resistance	Discovery	800		1200	Ω
$Z_{CBUS\_SINK\_ON}$	CBUS Pull Down Resistance	Active	90K		110K	Ω

DC Analogue Specifications (under normal operating conditions unless otherwise specified)

Symbol	Parameter	Conditions		Min	Typ	Max	Units
V_{OD}	Differential Voltage Single ended peak to peak amplitude	R_{LOAD} = 50 ohm R_{EXT_SWING} = 270 ohm		510	550	590	mV
V_{DOH}	Differential High-level Output Voltage[1]				AVCC		V
I_{DOS}	Differential Output Short Circuit Current	V_{OUT} = 0V; TX_TERM bit is 0				5	uA
I_{PD}	Power-Down Current[2]	25°C Ambient	3V3		40		uA
			1V8		5		uA
I_{CCD}	Supply Current (25°C Ambient, MHL Input R_{EXT_RES} = 510 ohm)	720p Resolution (8-bit)	3V3[3]		28		mA
			1V8		156		mA

1 Guaranteed by design.

2 Assumes all HDMI/DVI I/O ports are not connected and all digital inputs are silent.

3 Includes the current consumed by I/O pins and consumed by the receiver termination resistor

Receiver AC Specifications (under normal operating conditions unless otherwise specified)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
T_{DPS}	Intra-Pair (+ to -) Differential Input Skew[1]				0.4	T_{bit}
T_{CCS}	Channel to Channel Differential Input Skew[1]				1.0	T_{pixel}
T_{IJIT}	Differential Input Clock Jitter Tolerance[2,3]				0.3	T_{bit}
F_{MHL}	MHL Link CLK Frequency		25		75	MHz

NOTES:

1. Guaranteed by design.
2. Jitter defines as per DVI 1.0 Specification, Section 4.6 *Jitter Specification.*

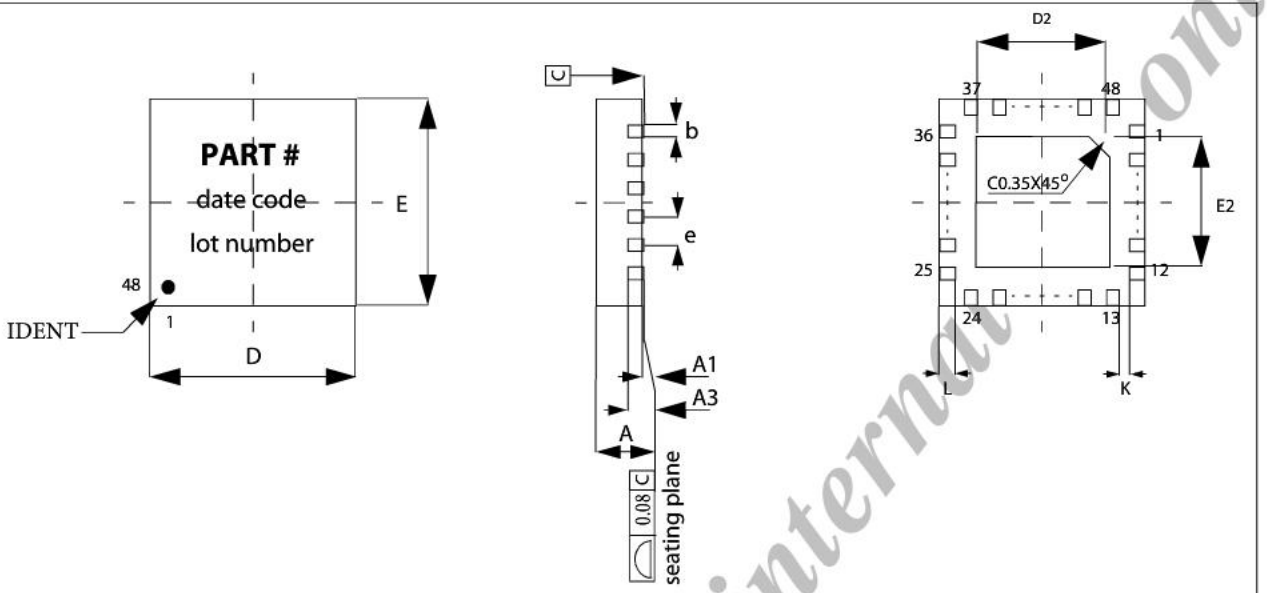
3. Jitter measured with Clock Recovery Unit as per DVI 1.0 Specification, Section 4.7 *Electronic Measurement Procedures*

Transmitter AC Specifications (under normal operating conditions unless otherwise specified)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
S_{LHT}	Differential Swing Low-to-High Transition Time	C_{LOAD} = 5pF, R_{LOAD} = 50 ohm	170	200	230	ps
S_{HLT}	Differential Swing High-to-Low Transition Time	C_{LOAD} = 5pF, R_{LOAD} = 50 ohm	170	200	230	ps

Appendix A Package

Figure A-1 QFN-48 Footprint Diagram



Footprint Variations (mm)

SYMBOLS	MIN.	NOM.	MAX.
A	0.80	0.85	0.90
A1	0.00	0.02	0.05
A3		0.20 REF	
b	0.20	0.25	0.30
D		7.00 BSC	
E		7.00 BSC	
D2	4.90	5.10	5.30
E2	4.90	5.10	5.30
e		0.50 BSC	
K	0.20	-	-
L	0.3	0.40	0.5

NOTES:
1. JEDEC OUTLINE : N/A
2. DIMENSION b APPLIES TO METALLIZED TERMINAL AND IS MEASURED BETWEEN 0.15mm AND 0.30mm FROM the TERMINAL TIP. IF THE TERMINAL HAS THE OPTIONAL RADIUS ON THE OTHER END OF THE TERMINAL, THE DIMENSION b SHOULD NOT BE MEASURED IN THAT RADIUS AREA.
3. THE MINIMUM "K" VALUE OF 0.2mm APPLIES.
4. BILATERAL COPLANARITY ZONE APPLIES TO THE EXPOSED HEAT SINK SLUG AS WELL AS THE TERMINALS.